

Timed Automata & Model Checking

Using UPPAALx : $x \in \{1,2,3,4\}$

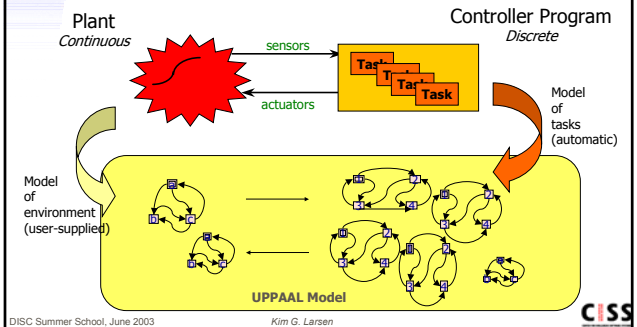
Kim Guldstrand Larsen
BRICS@Aalborg & FMT@Twente

BRICS
Basic Research
in Computer Science

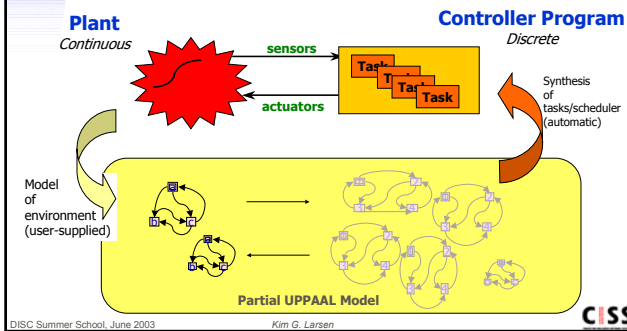
FMT
Formal methods
& Tools

CISS
CENTER FOR INNOVATIVE SOFTWARE SYSTEMS

Validation & Verification Construction of UPPAAL models

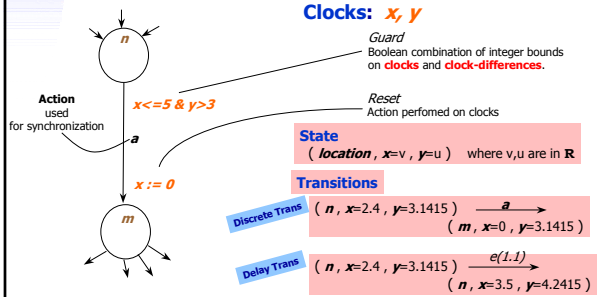


...and Beyond Synthesis of Control Program

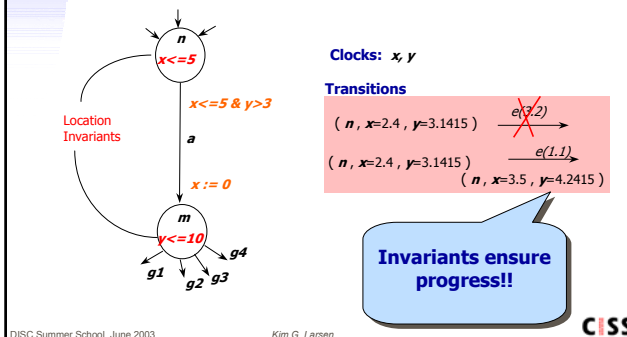


Timed Automata review

Alur & Dill 1990



Timed Automata review Invariants



Constraints

Definition

Let X be a set of clock variables. The set $B(X)$ of clock constraints ϕ is given by the grammar:

$$\phi ::= x \leq c \mid c \leq x \mid x < c \mid c < x \mid \phi_1 \wedge \phi_2$$

where $c \in \mathbb{N}$ (or \mathbb{Q}).

Clock Valuations and Notation

Definition

The set of *clock valuations*, \mathbb{R}^C is the set of functions $C \rightarrow \mathbb{R}_{\geq 0}$ ranged over by u, v, w, \dots

Notation

Let $u \in \mathbb{R}^C$, $r \subseteq C$, $d \in \mathbb{R}_{\geq 0}$, and $g \in \mathcal{B}(X)$ then:

- $u + d \in \mathbb{R}^C$ is defined by $(u + d)(x) = u(x) + d$ for any clock x
- $u[r] \in \mathbb{R}^C$ is defined by $u[r](x) = 0$ when $x \in r$ and $u[r](x) = u(x)$ for $x \notin r$.
- $u \models g$ denotes that g is satisfied by u .

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Timed Automata

Definition

A timed automaton A over clocks C and actions Act is a tuple (L, l_0, E, I) , where:

- L is a finite set of locations
- $l_0 \in L$ is the initial location
- $E \subseteq L \times \mathcal{B}(X) \times Act \times \mathcal{P}(C) \times L$ is the set of edges
- $I : L \rightarrow \mathcal{B}(X)$ assigns to each location an invariant

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Semantics

Definition

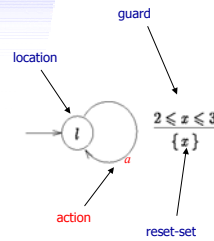
The semantics of a timed automaton A is a labelled transition system with state space $L \times \mathbb{R}^C$ with initial state $(l_0, u_0)^*$ and with the following transitions:

- $(l, u) \xrightarrow{\epsilon(d)} (l, u + d)$ iff $u \in I(l)$ and $u + d \in I(l)$,
- $(l, u) \xrightarrow{a} (l', u')$ iff there exists $(l, g, a, r, l') \in E$ such that
 - $u \models g$,
 - $u' = u[r]$, and
 - $u' \in I(l')$

* $u_0(x) = 0$ for all $x \in C$

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Timed Automata: Example

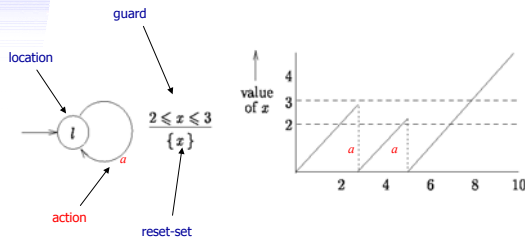


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Timed Automata: Example

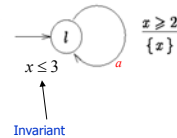


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Timed Automata: Example



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Timed Automata: Example

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Fundamental Results

Reachability ☺ Alur, Dill

Trace-inclusion Alur, Dill

Timed ☹ ; Untimed ☺

Bisimulation

Timed ☺ Cerans ; Untimed ☺

Model-checking ☺

TCTL, T_{mur} , L_{nur} , ...

PSPACE-c *EXPTIME-c*

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Updatable Timed Automata

	Diagonal-free	W Diagonals
$x := c, x := y$	Pspace complete	Pspace complete
$x := x + 1$		Undecidable
$x := y + c$		Undecidable
$x := x - 1$	Undecidable	Undecidable
$x < c, x \leq c$	Pspace complete	Pspace complete
$x > c, x \geq c$		Undecidable
$x \sim y + c$		Undecidable
$(y+c) < x < (y+d)$	Undecidable	Undecidable

With $\sim \in \{<, \leq, \geq, >\}$ and $c, d \in \mathbb{Q}_+$

	Diagonal-free	W Diagonals
$x := c, x := y$	TA-bisimilar	TA-bisimilar
$x := x + 1$		Turing
$x := y + c$		Turing
$x < c, x \leq c$	TA _c	TA _c
$x > c, x \geq c$		Turing
$x \sim y + c$		Turing
$(y+c) < x < (y+d)$	Turing	Turing

With $\sim \in \{<, \leq, \geq, >\}$ and $c, d \in \mathbb{Q}_+$

Patricia Bouyer, Catherine Dufourd, Emmanuel Fleury, Antoine Petit

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Other Extensions

- ✓ Ordinary clocks **x rate 1**
- ✓ Integer variables **x rate 0**
- ✓ Stopwatches **x rate 0** or **x rate 1** (*loc.dep.*)
- ✓ Cost **c rate n** where n is in \mathbb{N} , however c cannot be guarded
- + Const. slope clocks .. **x rate n** where n is in \mathbb{N}
- + Parameters **x rate 0** (and NOT assignable)
- + Multirate clocks
Lin. Hyb. Aut. **x rate [l,u]** where l, u is in \mathbb{N} linear guards & linear asgn.

Cassez, Larsen *HyTech*

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Parallel Composition (a'la CCS)

Example transitions

$(I1, m1, \dots, x=2, y=3.5, \dots) \xrightarrow{\text{tau}} (I2, m2, \dots, x=0, y=3.5, \dots)$

$(I1, m1, \dots, x=2.2, y=3.7, \dots)$

If a URGENT CHANNEL

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The UPPAAL Model

= Networks of Timed Automata + Integer Var + Array Var + ...

Example transitions

$(I1, m1, \dots, x=2, y=3.5, i=3, \dots) \xrightarrow{\text{tau}} (I2, m2, \dots, x=0, y=3.5, i=7, \dots)$

$(I1, m1, \dots, x=2.2, y=3.7, i=3, \dots)$

If a URGENT CHANNEL

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LEGO Mindstorms/RCX

- Sensors: temperature, light, rotation, pressure.
- Actuators: motors, lamps,
- Virtual machine:
 - 10 tasks, 4 timers, 16 integers.
- Several Programming Languages:
 - NotQuiteC, Mindstorm, Robotics, legOS, etc.

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First UPPAAL model

Sorting of Lego Boxes

Ken Tindell

Exercise: Design **Controller** so that only black boxes are being pushed out

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NQC programs

```

int active;
int DELAY;
int LIGHT_LEVEL;

task MAIN(
  DELAY=75;
  LIGHT_LEVEL=35;
  active=0;
  Sensor(IN_1, IN_LIGHT);
  Fwd(OUT_A,1);
  Display(1);

  start PUSH;

  while(true){
    wait(IN_1<=LIGHT_LEVEL);
    ClearTimer(1);
    active=1;
    PlaySound(1);
    wait(IN_1>LIGHT_LEVEL);
  }
}

task PUSH{
  while(true){
    wait(Timer(1)>DELAY && active==1);
    active=0;
    Rev(OUT_C,1);
    Sleep(8);
    Fwd(OUT_C,1);
    Sleep(12);
    Off(OUT_C);
  }
}

```

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UPPAAL Demo

IDA foredrag 20.4.99

From RCX to UPPAAL

- Model includes Round-Robin Scheduler.
- Compilation of RCX tasks into TA models.
- Presented at ECRTS 2000

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The Production Cell



Course at DTU, Copenhagen

Production Cell

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Case-Studies: Controllers


- Gearbox Controller [TACAS'98]
- Bang & Olufsen Power Controller [RTPS'99, FTRTFT'2k]
- SIDMAR Steel Production Plant [RTCSA'99, DSVW'2k]
- Real-Time RCX Control-Programs [ECRTS'2k]
- Experimental Batch Plant (2000)
- RCX Production Cell (2000)
- Terma, Memory Management for Radar (2001)

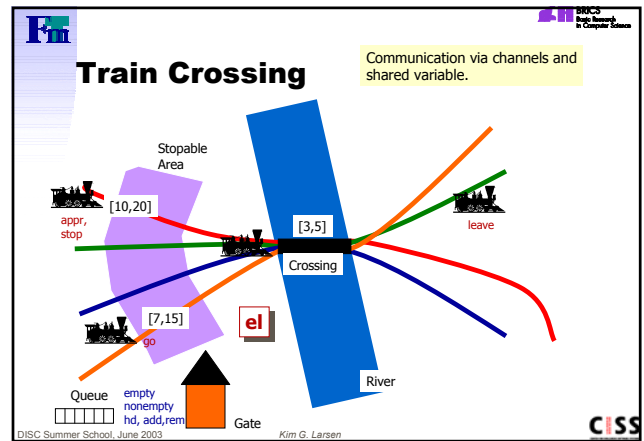
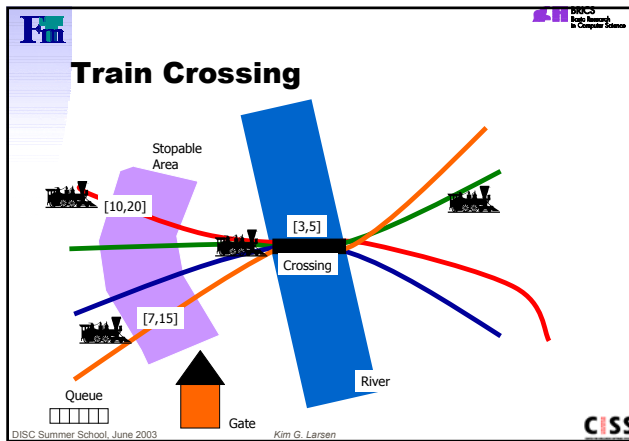
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Case Studies: Protocols

- Philips Audio Protocol [HS'95, CAV'95, RTSS'95, CAV'96]
- Collision-Avoidance Protocol [SPIN'95]
- Bounded Retransmission Protocol [TACAS'97]
- Bang & Olufsen Audio/Video Protocol [RTSS'97]
- TDMA Protocol [PRFTS'97]
- Lip-Synchronization Protocol [FMICS'97]
- Multimedia Streams [DSVIS'98]
- ATM ABR Protocol [CAV'99]
- ABB Fieldbus Protocol [ECRTS'2k]
- IEEE 1394 Firewire Root Contention (2000)

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




UPPAAL 3.2 (and 3.3, 3.4)

Released October 01

- Graphical User Interface www.uppaal.com
 - XML based file format
 - Better syntax-error indication
 - Drop-and-drag for transitions
 - Changed menu
- Verification Engine
 - Restructured (increased flexibility)
 - Normalization-bug fixed
 - More freedom in combining optimization options
 - Deadlock checking
 - Support for more general properties ($E[]p$, $A<>p$, $p \rightarrow q$)

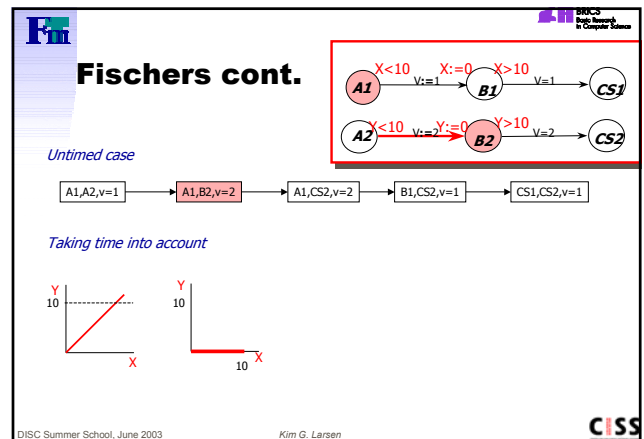
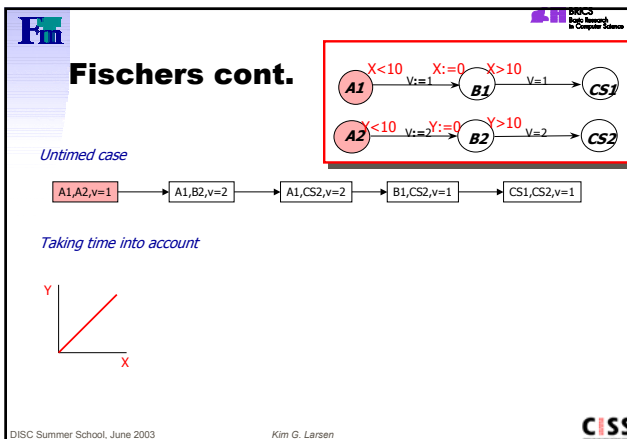
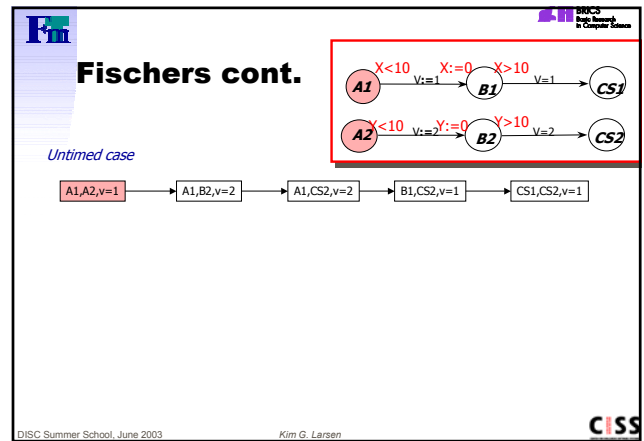
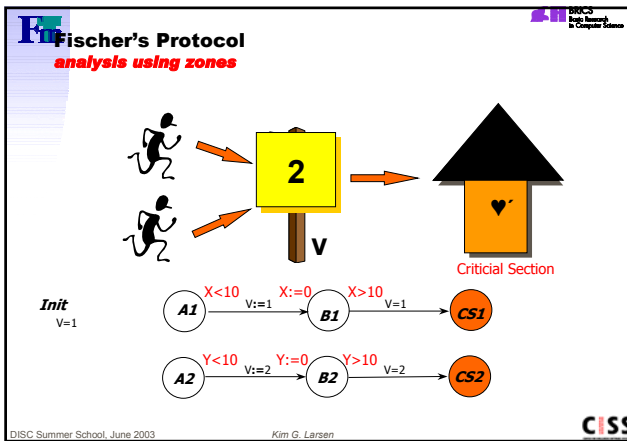
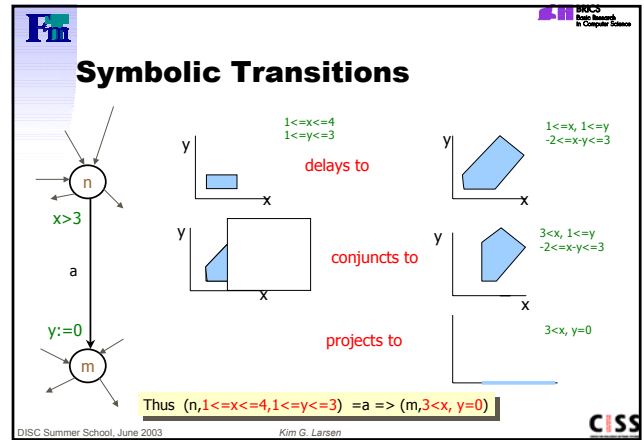
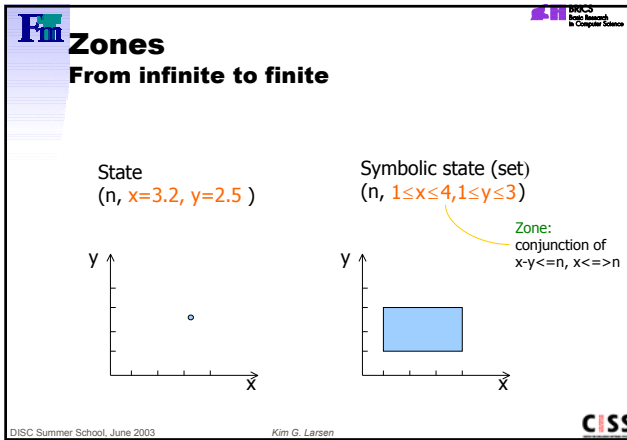
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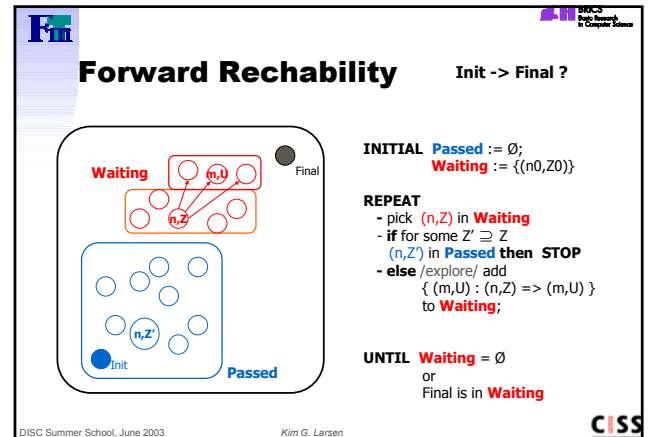
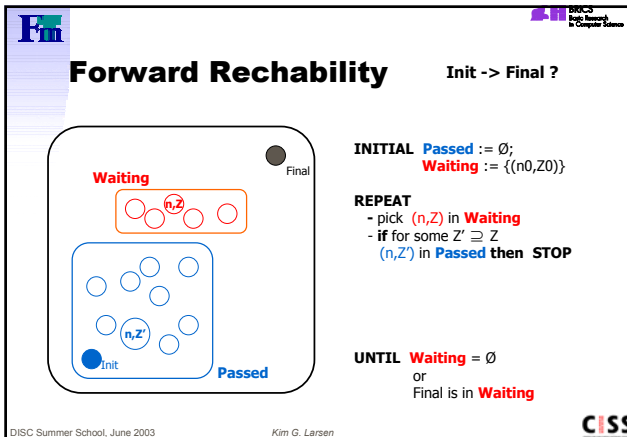
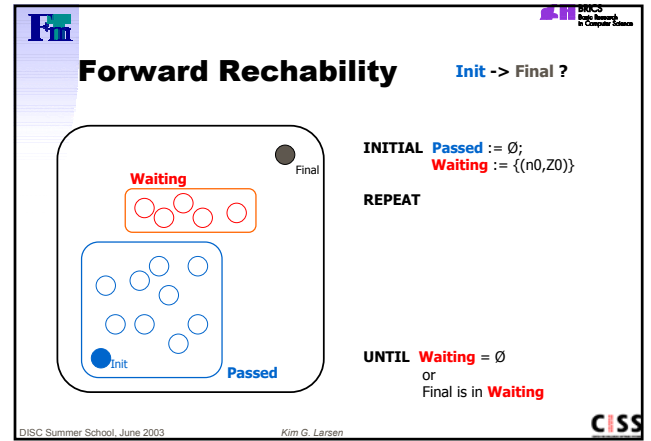
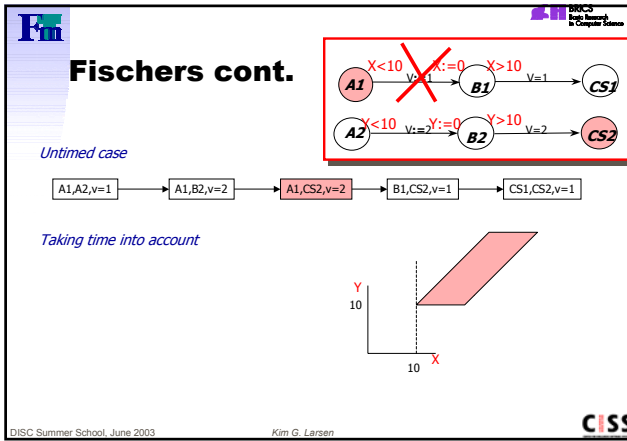
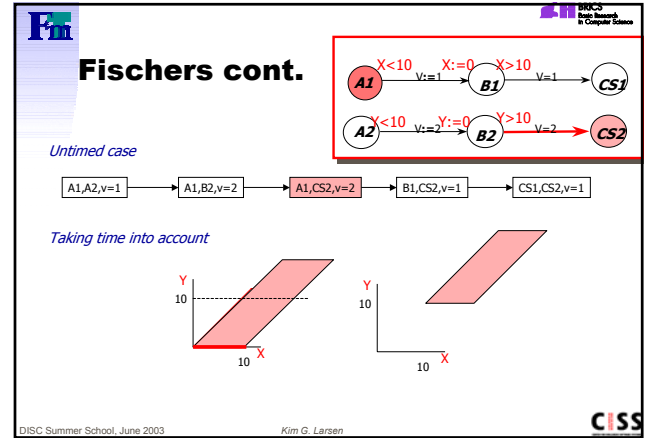
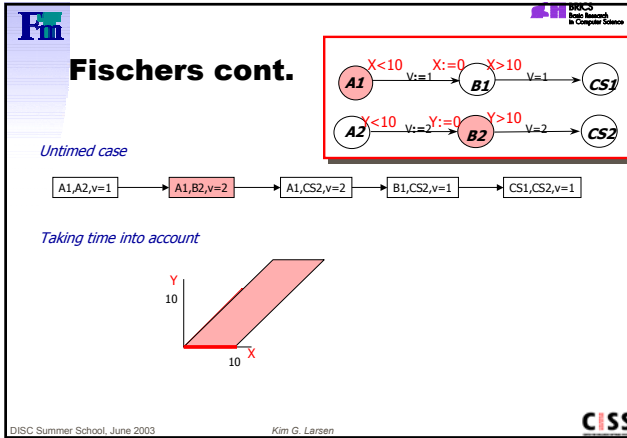



THE UPPAAL ENGINE

**Symbolic
Reachability
Checking**

IDA foredrag 20.4.99





Forward Reachability

Init -> Final ?

INITIAL **Passed** := \emptyset ;
Waiting := $\{(n, Z)\}$

REPEAT
 - pick (n, Z) in **Waiting**
 - if for some $Z' \supseteq Z$ (n, Z') in **Passed** then **STOP**
 - else /explore/ add $\{(m, U) : (n, Z) \Rightarrow (m, U)\}$ to **Waiting**;
 Add (n, Z) to **Passed**

UNTIL **Waiting** = \emptyset
 or
 Final is in **Waiting**

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Canonical Datastructures for Zones

Difference Bounded Matrices Bellman 1958, Dill 1989

Inclusion

D1 $\begin{cases} x \leq 1 \\ y - x \leq 2 \\ z - y \leq 2 \\ z \leq 9 \end{cases}$ Graph

D2 $\begin{cases} x \leq 2 \\ y - x \leq 3 \\ y \leq 3 \\ z - y \leq 3 \\ z \leq 7 \end{cases}$ Graph

$? \subseteq ?$

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Canonical Datastructures for Zones

Difference Bounded Matrices Bellman 1958, Dill 1989

Inclusion

D1 $\begin{cases} x \leq 1 \\ y - x \leq 2 \\ z - y \leq 2 \\ z \leq 9 \end{cases}$ Graph Shortest Path Closure

$? \subseteq ?$

D2 $\begin{cases} x \leq 2 \\ y - x \leq 3 \\ y \leq 3 \\ z - y \leq 3 \\ z \leq 7 \end{cases}$ Graph Shortest Path Closure

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Canonical Datastructures for Zones

Difference Bounded Matrices Bellman 1958, Dill 1989

Emptiness

D $\begin{cases} x \leq 1 \\ y \geq 5 \\ y - x \leq 3 \end{cases}$ Graph

Negative Cycle
 iff
 empty solution set

Compact

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Canonical Datastructures for Zones

Difference Bounded Matrices

Future

D $\begin{cases} 1 \leq x \leq 4 \\ 1 \leq y \leq 3 \end{cases}$ **Future D** $\begin{cases} 1 \leq x, 1 \leq y \\ -2 \leq x - y \leq 3 \end{cases}$

Shortest Path Closure

Remove upper bounds on clocks

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Canonical Datastructures for Zones

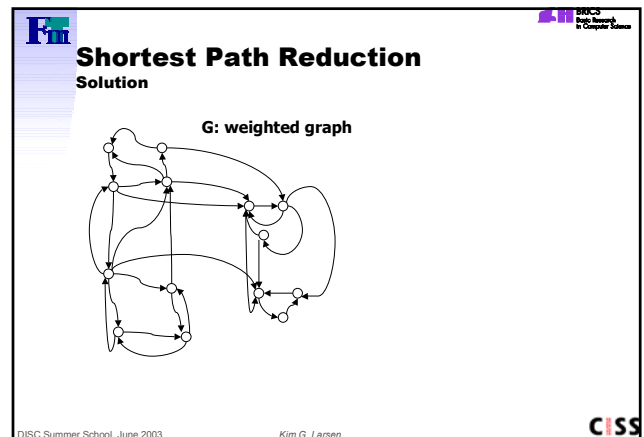
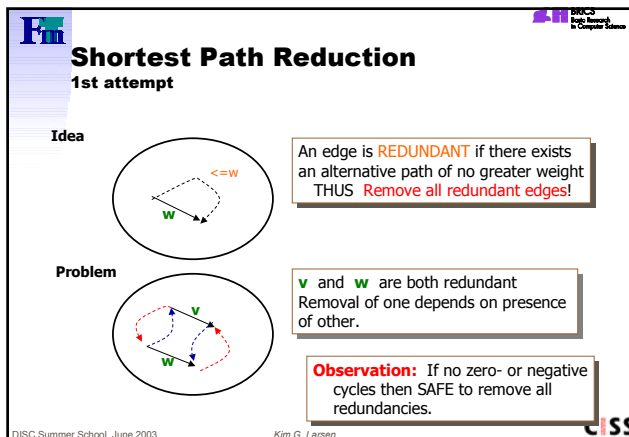
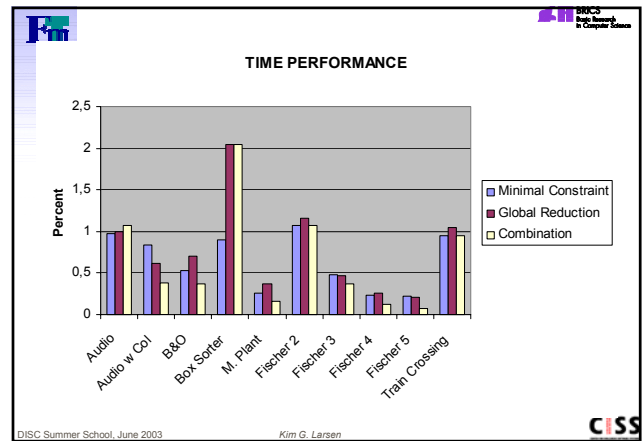
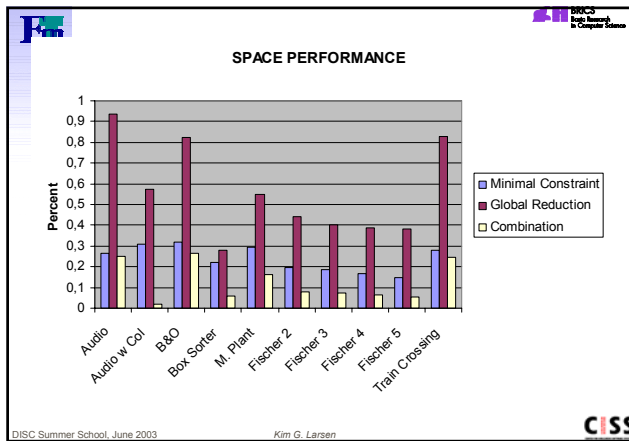
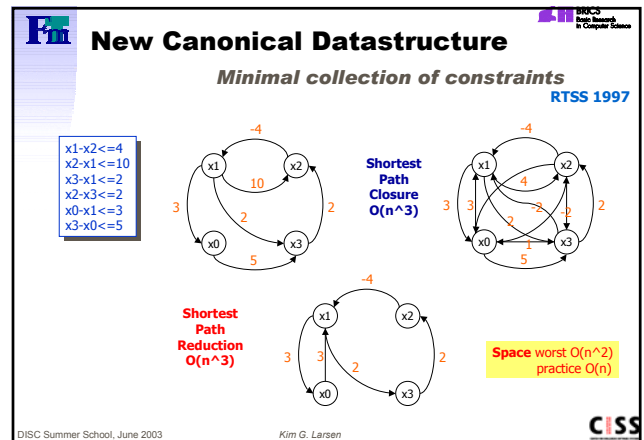
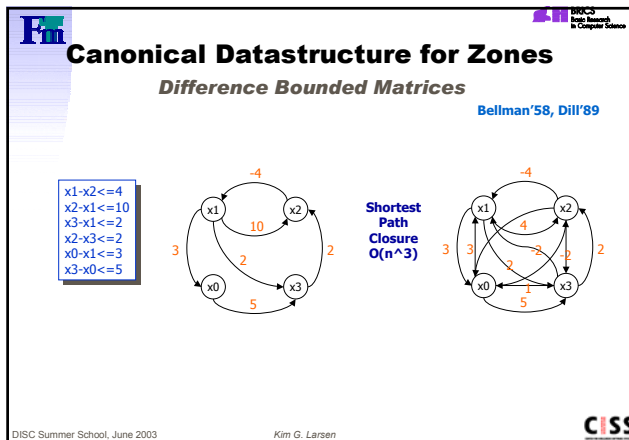
Difference Bounded Matrices



Reset

D $\begin{cases} 1 \leq x, 1 \leq y \\ -2 \leq x - y \leq 3 \end{cases}$ **{y}D** $\begin{cases} y = 0, 1 \leq x \end{cases}$

Remove all bounds involving y and set y to 0

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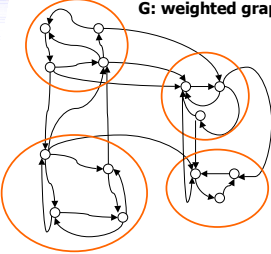


Shortest Path Reduction



Solution

G: weighted graph



1. Equivalence classes based on 0-cycles.

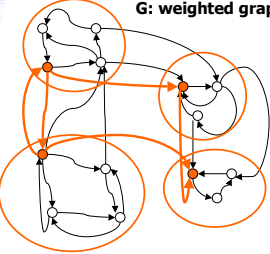
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Shortest Path Reduction



Solution

G: weighted graph



1. Equivalence classes based on 0-cycles.
2. Graph based on **representatives**. Safe to remove redundant edges

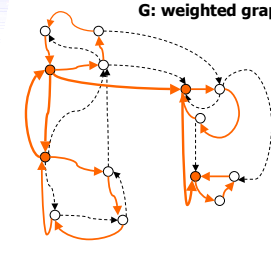
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Shortest Path Reduction

Solution



G: weighted graph



1. Equivalence classes based on 0-cycles.
2. Graph based on **representatives**. Safe to remove redundant edges
3. **Shortest Path Reduction**
= One cycle pr. class + Removal of redundant edges between classes

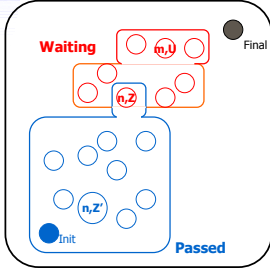
Canonical given order of clocks

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Earlier Termination

Init -> Final ?





INITIAL **Passed** := \emptyset ;
Waiting := $\{(n_0, Z_0)\}$

REPEAT

- pick (n, Z) in **Waiting**
- if for some $Z' \supseteq Z$ (n, Z') in **Passed** then **STOP**
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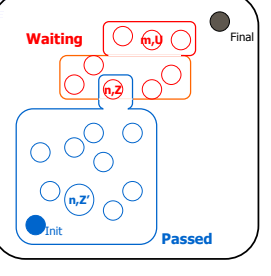
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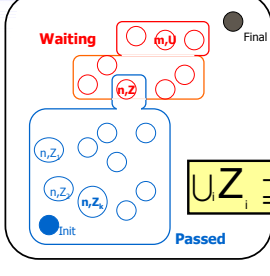
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Earlier Termination

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Add (n, Z) to **Passed**

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Clock Difference Diagrams

= Binary Decision Diagrams + Difference Bounded Matrices

CAV99

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CDD-representations

(a)

(b)

- Nodes labeled with differences
- Maximal sharing of substructures (also across different CDDs)
- Maximal intervals
- Linear-time algorithms for set-theoretic operations.

(c)

- NDD's Maler et. al
- DDD's Möller, Lichtenberg

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SPACE PERFORMANCE

Benchmark	CDD (%)	Reduced CDD (%)	CDD+BDD (%)
Philips	1.0	1.0	3.8
Philips col	0.5	0.5	2.0
B&O	0.5	0.5	0.8
BRP	0.2	0.2	0.3
PowerDown1	0.5	0.5	1.2
PowerDown2	1.0	1.0	1.2
Dacapo	0.5	0.5	1.5
GearBox	0.5	0.5	4.2
Fischer4	0.8	0.8	0.8
Fischer5	1.5	1.5	1.5

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TIME PERFORMANCE

Benchmark	CDD (%)	Reduced CDD (%)	CDD+BDD (%)
Philips	1.0	1.0	1.8
Philips col	1.0	1.0	3.2
B&O	1.0	1.0	5.2
BRP	1.0	1.0	3.2
PowerDown1	1.0	1.0	2.0
PowerDown2	1.0	1.0	4.2
Dacapo	1.0	1.0	4.8
GearBox	1.0	1.0	2.8
Fischer4	1.0	1.0	2.2
Fischer5	1.0	1.0	3.8

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UPPAAL 1995 - 2001

Dec %

Every 9 month
10 times better
performance!

3.x

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